Remarks/Arguments

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-13 and 19 are presently active. Claims 1, 5, 6, 9, 10, and 13 have been amended and Claim 19 added by the present amendment. Claims 14-18 have been withdrawn.

In the Office Action dated Oct. 29, 2002, Claims 1-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,019,527 to Ohshima et al. (hereinafter "the '527 patent") in view of U.S. Patent No. 5,482,894 to Havemann (hereinafter "the '894 patent").

The above change to the specification is made to clarify the order of processing consistent with the original disclosure, and is not believed to raise a question of new matter.

Next, Applicants acknowledge with appreciation the courtesy of the interview granted to Applicants' attorney on June 12, 2003, at which time the outstanding issues in this case were discussed. During the interview, the above changes to Claims 1, 5, 6, 9, 10, and 13 were proposed, and arguments substantially as hereinafter developed were presented. No agreement was reached, pending the Examiner's reconsideration of the application upon formal submission of the amendment.

As discussed during the interview, amended Claim 1 is directed to a semiconductor memory device comprising, *inter alia*, (1) a semiconductor body of a first conductivity type; (2) a stack gate formed on the semiconductor body; (3) a contact material buried to be adjacent to the first side surface of the stack gate; (4) a first insulating film formed on the second side surface and on the upper surface of the stack gate; and (5) a second insulating

film formed on the first side surface adjacent to the contact material, the second insulating film covering the entirety of the first insulating film. The active independent claims have been amended to clarify that the second insulating film formed on the first side surface adjacent to the contact material has an etch rate slower than that of said first insulating film, consistent with the preferred materials stated in e.g. in Claim 5 and the reference to etching selection ratio stated at page 23, line 24 of the specification. No new matter has been added.

Also, new Claim 19 is submitted herewith and specifically recites that the first and second insulating films are made of a silicon oxide film and a silicon nitride film, respectively. No new matter is added by Claim 19.

As discussed during the interview, Applicants' invention addresses several problems existing in the conventional non-volatile semiconductor memory device, as discussed in Applicants' specification. A first problem described at pages 7 and 8 of the specification arises due to the application of a silicon-nitride-based film to cover the gate structure of the transistor, resulting in a stack insulating film structure constructed by a gate film mainly made of a silicon dioxide film and a silicon nitride film formed on the diffusion layer on the side of the gate structure opposite the contact side. This creates a parasitic capacitance by which "hot electrons" generated at channels during operation of a pentode of a transistor are caught by the inter-layer insulating film interface (the interface between the gate insulating film and the silicon nitride film), causing an electron trap. Problems associated with such an electron trap, as described at page 8, lines 1-5 of the specification, thereby occur.

To solve the "hot electrons" problems, a structure in which a silicon-dioxide-based film is sandwiched between the silicon nitride film and the gate has been proposed. The object of sandwiching a silicon-dioxide-based film between a thin gate insulating film on a

diffusion layer and a silicon nitride film is to widen the distance between the diffusion layer and the silicon nitride film to reduce caught hot electrons.[1] However, the introduction of a two-layer insulating film structure to solve the "hot electrons" problem associated with the single layer silicon nitride insulating film as a result of another problem of reduced yield. Applicants have determined the source of the yield problem arises in that during etching of the contact hole for the contact 217 shown in Figure 4A, for example, part of the silicon oxide layer 214 is etched back, and as a result, as shown in Figure 4B, the contact material 217 (buried-electrode material) enters into the etched-back part of the silicon dioxide layer 214 so that the possibility of short-circuiting between the contact material 217 and the control gate 205 rises.[2]

Applicants' invention, when considered on the whole, includes not only the recognition of the source of the yield problem, i.e., the short-circuit arising due to overlapping insulating layers on the contact side of the gate structure where the upper insulating layer has an etching rate slower than that of the lower layer, but also the solution thereto, i.e., the structure, for example, as shown in Figure 8B in the example of the NAND-type memory cell, wherein the stacked gate of the memory cell is covered with the gate barrier film 42, preferably oxide based (Claims 5), and the gate barrier film 42 is covered with the contact barrier film 43, preferably nitride based (Claim 5), and in which the stacked gate of the selection transistor has a structure in which the side surface adjacent to the contact material 38 or 39 is not covered with the gate barrier film 42, but is directly covered with the contact barrier film 43. In other words, the contact side of the selection transistor gate structure is

[1]Specification, paragraph linking pages 8 and 9.

[2]Id., page 10, lines 16-21.

covered only with a single contact barrier film 43, having an etching rate slower than that of the gate barrier film 42, whereas the opposite side of the selection transistor gate structure is covered by a two-layer insulating combination of the gate barrier film 42 covered by the contact barrier film 43.

Thus, as explained in Applicants' specification, in the claimed device, the gate barrier film 42 is not formed on the side surface of the stacked gate, which is adjacent to the bit-line contact material 38, when forming a contact hole at the bit-line contact material 38 (or the common source line contact material 39) having a self-aligned contact structure. Therefore, the contact material does not enter into the cavity area where the gate barrier film is etched, and it is thus possible to prevent the contact material in the control gate from being short-circuited.[3]

Further, the gate barrier film (preferably oxide based) 42 is formed between the gate insulating film 32 and both sides of the stacked gate of the memory cell (on the n-type diffusion layer 37 forming a source or drain) and the contact barrier film (preferably nitride based) 43. Therefore, it is possible to reduce hot carriers caught between the gate insulating film 32 and the contact barrier film 43. The electric characteristics of the memory can hence be prevented from being changed due to influences from caught hot carriers.[4]

As discussed during the interview, the present amendment to the independent Claims 1, 5, 6, 9, 10, and 13 to state that the second insulating layer has an etching rate slower than the first insulating layer addresses the short-circuit problem recognized and solved according

[3]Id., page 31, line 20 - page 32, line 5.

[4]Id., page 32, lines 6-15.

to Applicants' invention. This is likewise true of the silicon oxide and silicon nitride films stated in new Claim 19.

Turning now to the applied Ohshima et al. patent, Ohshima et al. disclose a method of manufacturing non-volatile semiconductor memories and is relied upon in the outstanding rejection for its processing steps shown in Figures 8A-8I. As there shown, however, the structure disclosed by Ohshima et al. results in a silicon dioxide contact-side spacer 11 in a silicon dioxide insulating film 12 covering the opposite or second side surface and top surface, but not the contact-side first side surface. As is readily evident by inspection, compared to the claimed invention, the structure shown in Figure 8I of the Ohshima et al. patent is a very different gate structure in which single insulation layers cover the contact sides of the gate structure adjacent to contact material 24. Not only are the problems addressed by Applicants' invention not recognized in the Ohshima et al. patent, but also the structure of the insulating layers covering the gate structure as taught by Ohshima et al. is quite different from that claimed. Clearly, there is no discussion in Ohshima et al. in regard to etching rates or the reason for having different insulating layers with different etching rates covering the gate structure. For these reasons, it is respectfully submitted that Ohshima et al. at most includes isolated teachings which in no way suggest Applicants' claimed invention.

Havemann in Figures 2D and 3 disclosed a self-aligned contact on the semiconductor device. In Figure 2D, an insulating layer 30, described in the Table at column 6 as preferably being a CVD oxide or alternatively as CVD oxide, silicon nitride or silicon oxynitride, is covered by an insulating film 42, described in the Table at column 6 as preferably being silicon nitride or alternatively a thermal oxide or CVD oxide. Havemann's teaching of the preferred materials for insulating layer 32, i.e., a thermally-grown oxide, and for insulation

layer 42, i.e., a silicon nitride film, results in a device having the contact side surface of the gate structure shown in Figure 2D, which is susceptible to the problem of etch-through and short-circuiting of the gate. Thus, it is clear that Havemann in no way recognizes the short-circuit problem addressed by Applicants' invention and the solution thereto as claimed.

On the other hand, in the Havemann embodiment shown in Figure 3, the two layer insulating structure shown in Figure 2D is discarded in favor of a single insulating layer 30, disclosed as being preferably a thermally-grown oxide and alternatively, for example, a silicon nitride as described in the table provided at column 6. This single layer approach contradicts the dual layer approach shown in Figure 2 of Havemann and in no way suggests a single silicon nitride contact side insulating layer covering a contact side insulating gate structure directly, and covering a silicon oxide layer on the opposite side of the gate structure. Further, there is no disclosure as to any relative etching rate of two insulating layers, as claimed. Once again, like the Ohshima et al. patent, Havemann provides no coherent pattern of teachings which would lead a person skilled in the art to the claimed structure by which the above-discussed problems are solved.

Finally, Applicants address the motivation noted in the Official Action dated October 29, 2002, that "Havemann teaches (e.g., Figures 2C and 2D) to form a second insulating film 42 on said first side surface and with contact material 40 having a side surface and contact with the second insulating film and covering the entirety of the first insulating film to provide minimal protection during O_2 plasma etch (column 5, lines 16-31)."[5] This statement in the outstanding rejection seems to indicate that Havemann is relied upon for teaching protection of the gate side wall during etching. However, the precise teaching of Havemann is "**to**

[5]Official Action dated October 29, 2000, last paragraph.

provide a minimal protection for substrate 20 during O_2 plasma etch to remove organic containing material from insulting gap 29."[6] (Emphasis added) To protect the substrate 20, **NOT** the gate structure side wall, therefore, Havemann teaches provision of the dielectric overlayer 42 on both sides of the gate structure, not just on the contact side structure. Far from motivating a derivation of the claimed invention, the teaching relied upon in fact teaches away from the claimed invention, and even then, Havemann at column 5, lines 17 and 18, teaches that either a thermal oxide or a silicon nitride layer can be used, which again teaches away from the etching selectivity stated in the amended independent claims. Therefor, it is respectfully submitted that it could only be through a hindsight reconstruction of Applicants' invention by which the teachings of the applied prior art can be manipulated to derive the claimed invention. Accordingly, it is respectfully submitted that the outstanding grounds for rejection are traversed.

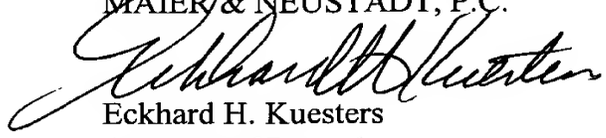
Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and

[6]Havemann, column 5, lines 18-20.

favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,830

22850

(703) 413-3000
Fax #: (703) 413-2220
EHK/cja
I:\ATTY\EHK\AMEND-RESPONSES\0039\212706US-AM1-RCE.DOC